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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LAZARO, DAVID R	

ART UNIT	PAPER NUMBER
2155	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/674,939	TOURANCHEAU, BERNARD	
	Examiner	Art Unit	
	David Lazaro	2155	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed 10/29/2007.

2. Claims 1, 8 and 15 were amended.

3. Claims 1-21 are pending in this office action.

Response to Amendment

4. The objections to claim 1 and 8 are withdrawn based on the amendment.

5. Applicant's arguments filed 10/29/2007 have been fully considered but they are not persuasive. Please see Response to Arguments. Accordingly, the grounds of rejection as presented in the 08/09/2007 office action are respectfully maintained.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,973,517 by Golden et al. (Golden).

8. With respect to claims 1 and 8, Golden teaches an apparatus (and corresponding method for a computer system) for routing data between integrated circuit devices, comprising:

an n-dimensional grid of integrated circuit devices (Col. 6 lines 43-58, Col. 7 lines 8-26, Col. 61-66: multiprocessor mesh configuration which include integrated circuit devices);

a plurality of communication networks coupling the n-dimensional grid of integrated circuit devices, wherein a communication network of the plurality of communication networks moves data unidirectionally in only orthogonal dimensions (Col. 6 lines 43-58 and Col. 10 line 56 - Col. 11 line 11: "cycles eliminated if messages route all in one dimension before routing any in the next dimension" and dimension order routing); and

a routing mechanism configured to route data across the plurality of communication networks as well as into, out of, and through a given integrated circuit within the n-dimensional grid of integrated circuits (Col. 6 lines 43-58 and Col. 10 line 56 - Col. 11 line 11);

whereby a process of routing signals across a given communication network is greatly simplified because it is not possible to create a cycle that causes a deadlock within the given communication network (Col. 10 line 56 - Col. 11 line 11: dimension order routing prevents deadlock); and

whereby the process of routing signals yields a shortest path between source and destination (Col. 10 line 56 - Col. 11 line 11: minimal adaptive routing yields shortest path).

9. With respect to claims 2 and 9, Golden teaches all the limitations of claims 1 and 8 respectively and further teaches wherein the n-dimensional grid of integrated circuit devices includes memory devices (Col. 7 lines 8-32).

10. With respect to claims 3 and 10, Golden teaches all the limitations of claims 1 and 8 respectively and further teaches wherein the n-dimensional grid of integrated circuit devices includes processor devices (Col. 6 lines 43-58), I/O devices (Col. 7 lines 8-26), digital signal processors (Col. 7 lines 8-26 and Col. 8 lines 43-66), field programmable gate arrays (Col. 7 lines 32-46), sensors (Col. 16 lines 15-32), and controllers (Col. 7 lines 8-32 and Col. 8 lines 59-66).

11. With respect to claims 4 and 11, Golden teaches all the limitations of claims 1 and 8 respectively and further teaches wherein the plurality of communication networks for a two-dimensional grid includes: a first communication network configured to move signals East and North; a second communication network configured to move signals North and West; a third communication network configured to move signals West and South; and a fourth communication network configured to move signals South and East (Col. 6 lines 43-58 and Col. 10 line 56 - Col. 11 line 11).

12. With respect to claims 5 and 12, Golden teaches all the limitations of claims 1 and 8 respectively and further teaches wherein the routing mechanism is configured to

statically route data items across the plurality of communication networks (Col. 11 lines 5-49: deadlock-free network).

13. With respect to claims 6 and 13, Golden teaches all the limitations of claims 1 and 8 respectively and further teaches wherein the routing mechanism is configured to dynamically route data items through network junctions within each integrated circuit (Col. 11 lines 5-49: adaptive routing).

14. With respect to claims 7 and 14, Golden teaches all the limitations of claims 1 and 8 respectively and further teaches wherein a header attached to each data item in a two-dimensional grid indicates a number of horizontal steps and a number of vertical steps required for the data item to reach its destination (Col. 11 lines 50-67); and wherein during a dynamic routing process, the routing mechanism removes a horizontal step or a vertical step from the header for the data item, depending upon which direction is dynamically selected (Col. 11 lines 50-67).

15. With respect to claim 15, Golden teaches a means for routing data between integrated circuit devices within an n-dimensional grid of integrated circuit devices, comprising:

a communication means comprising a plurality of communication networks coupling the n-dimensional grid of integrated circuit devices (Col. 6 lines 43-58, Col. 7 lines 8-26, Col. 61-66: multiprocessor mesh configuration which include integrated circuit devices), wherein a communication network of the plurality of communication networks moves data unidirectionally in only orthogonal dimensions (Col. 6 lines 43-58

and Col. 10 line 56 - Col. 11 line 11: "cycles eliminated if messages route all in one dimension before routing any in the next dimension" and dimension order routing); and

a routing means for routing data across the plurality of communication networks as well as into, out of, and through a given integrated circuit within the n-dimensional grid of integrated circuits (Col. 6 lines 43-58 and Col. 10 line 56 - Col. 11 line 11);

whereby the means of routing signals yields a shortest path between source and destination (Col. 10 line 56 - Col. 11 line 11: minimal adaptive routing yields shortest path).

16. With respect to claim 16, Golden teaches all the limitations of claim 15 and further teaches wherein the n-dimensional grid of integrated circuit devices includes memory devices (Col. 7 lines 8-32).

17. With respect to claim 17, Golden teaches all the limitations of claim 15 and further teaches wherein the n-dimensional grid of integrated circuit devices includes processor devices (Col. 6 lines 43-58), I/O devices (Col. 7 lines 8-26), digital signal processors (Col. 7 lines 8-26 and Col. 8 lines 43-66), field programmable gate arrays (Col. 7 lines 32-46), sensors (Col. 16 lines 15-32), and controllers (Col. 7 lines 8-32 and Col. 8 lines 59-66).

18. With respect to claim 18, Golden teaches all the limitations of claim 15 and further teaches wherein the plurality of communication networks for a two-dimensional grid includes: a first communication network configured to move signals East and North; a second communication network configured to move signals North and West; a third communication network configured to move signals West and South; and a fourth

communication network configured to move signals South and East (Col. 6 lines 43-58 and Col. 10 line 56 - Col. 11 line 11).

19. With respect to claim 19, Golden teaches all the limitations of claim 15 and further teaches wherein data is configured to statically routed across the plurality of communication networks (Col. 11 lines 5-49: deadlock-free network).

20. With respect to claim 20, Golden teaches all the limitations of claim 15 and further teaches wherein data is dynamically routed through network junctions within each integrated circuit (Col. 11 lines 5-49: adaptive routing).

21. With respect to claim 21, Golden teaches all the limitations of claim 15 and further teaches wherein a header attached to each data item in a two-dimensional grid indicates a number of horizontal steps and a number of vertical steps required for the data item to reach its destination (Col. 11 lines 50-67); and wherein during a dynamic routing process, a horizontal step or a vertical step is removed from the header for the data item, depending upon which direction is dynamically selected (Col. 11 lines 50-67).

Response to Arguments

22. Applicant's arguments filed 10/29/2007 have been fully considered but they are not persuasive.

23. Applicant argues on page 9 of the remarks - "*In contrast, embodiments of the present invention include separate networks the move data* ***unidirectionally in only orthogonal dimensions*** *(see instant application, par. [0028]).*"

a. Examiner's response - Golden explicitly states in col. 10 line 63 to col. 11 line 1, "These cycles can be eliminated if messages route all in one dimension before routing any in the next dimension or in dimension order. For example, if all messages traversed in the East-West (EW) direction before traversing in the North-South (NS) direction, no deadlock cycles can be generated...". The examiner considers this to be within the scope of "unidirectionally in only orthogonal dimensions". Applicant's arguments are not persuasive.

24. Applicant argues on page 10 of the remarks - "*However, Golden's deadlock free adaptive routing requires an "adaptive network of buffers" coupled to a "deadlock free network"...*"

b. Examiner's response - Each of the independent claims uses the wording "comprising", thus leaving the subject matter open ended. As such, the claims do not restrict additional elements such as an "adaptive network of buffers" coupled to a "deadlock free network". Applicant's arguments are not persuasive.

Conclusion

25. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Lazaro whose telephone number is 571-272-3986. The examiner can normally be reached on 8:30-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Saleh Najjar can be reached on 571-272-4006. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

David Lazaro
January 7, 2008

SALEH NAJJAR
SUPERVISORY PATENT EXAMINER